What is Claimed is:

1. A method for producing a gate structure for an MOS transistor, comprising:

generating a layer sequence of an oxide layer, an auxiliary layer and a masking layer on a substrate, wherein the auxiliary layer and the masking layer are structured to determine an edge separating an area of the oxide layer covered with these layers from an exposed area thereof;

performing an oxidation to generate an oxide ramp in the area of the edge;

partly removing the auxiliary layer to generate a hollow space of a predetermined length between the oxide layer and the masking layer; and

introducing a gate electrode material into the hollow space to generate a gate electrode.

2. The method according to claim 1, wherein the substrate comprises a silicon substrate, the oxide layer comprises a silicon oxide layer, the auxiliary layer comprises a silicon nitride layer and the masking layer comprises a silicon oxide layer.

3. The method according to claim 1, wherein the gate electrode material comprises polysilicon.

4. The method according to claim 1, further comprising the step of removing an oxide formed during the oxidation on a sidewall of the auxiliary layer, which is located at the edge, prior to partly removing the auxiliary layer.

5. The method according to claim 4, wherein the oxide on the sidewall of the auxiliary layer is removed by an oxide etching.

6. The method according to claim 1, wherein the auxiliary layer is etched back selectively wet-chemically for generating the hollow space.

7. The method according to claim 1, wherein introducing the gate electrode material into the hollow space comprises:

depositing a gate electrode material layer on the structure present after generating the hollow space, wherein the hollow space is also filled in with the gate electrode material; and

anisotropically and selectively back-etching the gate electrode material layer outside the hollow space filled with gate electrode material.

8. The method according to claim 1, further comprising a step of removing at least the masking layer for exposing the gate electrode.

9. The method according to claim 8, wherein the step of removing at least the masking layer comprises a step of anisotropically and selectively back-etching the masking layer.

10. The method according to claim 8, further comprising a step of anisotropically and selectively back-etching the auxiliary layer.

11. A method for producing a gate structure for an MOS transistor, comprising:

generating a structure on a substrate, the structure having at least an oxide layer and a masking layer, the masking layer disposed over a part of the oxide layer, the oxide layer including an oxide ramp, the masking layer including an inclined edge disposed above the oxide ramp, the structure further including a hollow space between the oxide layer and the masking layer; and

introducing a gate electrode material into the hollow space to generate a gate electrode.

12. The method according to claim 11, wherein the substrate comprises a silicon substrate, the oxide layer comprises a silicon oxide layer, and the masking layer comprises a silicon oxide layer.

13. The method according to claim 11, wherein the gate electrode material comprises polysilicon.

14. The method according to claim 11, wherein generating the structure on the substrate, further comprises providing a partial auxiliary layer disposed between the oxide layer and the masking layer and adjacent to the hollow space.

15. The method according to claim 11, wherein generating the structure on the substrate further comprises forming the hollow space by removing material from an auxiliary layer, the auxiliary layer including the partial auxiliary layer.

16. The method according to claim 15, wherein the auxiliary layer is etched back selectively wet-chemically to generate the hollow space.

17. The method according to claim 11, wherein introducing the gate electrode material into the hollow space comprises:

depositing a gate electrode material layer on the structure present after generating the hollow space, wherein the hollow space is also filled in with the gate electrode material; and

anisotropically and selectively back-etching the gate electrode material layer outside the hollow space filled with gate electrode material.

18. The method according to claim 11, further comprising a step of removing at least the masking layer for exposing the gate electrode.

19. The method according to claim 18, wherein the step of removing at least the masking layer comprises a step of anisotropically and selectively back-etching the masking layer.

20. The method according to claim 18, wherein generating the structure on the substrate further comprises providing a partial auxiliary layer disposed between the oxide layer and the masking layer and adjacent to the hollow space, the method further comprising a step of anisotropically and selectively back-etching the auxiliary layer.